

5           **DIGITAL DEMODULATION AND APPLICATIONS THEREOF**

**TECHNICAL FIELD OF THE INVENTION**

10           This invention relates generally to wireless communication and in particular to digital demodulation within wireless radio receivers.

15           **BACKGROUND OF THE INVENTION**

20           The use of wireless communication for in-home, in-building networks and point-to-point communications is increasing in popularity and spawning relatively new standards including, but not limited to Bluetooth, IEEE 802.11a, and IEEE 802.11b. As is known for wireless communications, data is modulated on to at least one radio frequency (RF) carrier frequency and transmitted as a RF modulated signal by a radio transmitter. A radio receiver  
25 receives the RF modulated signal and demodulates it to recapture the data.

30           As is further known, there are a variety of modulation/demodulation protocols that may be used for wireless communications. Such modulation/demodulation protocols include amplitude modulation (AM), frequency modulation (FM), amplitude shift-keying (ASK), frequency shift-keying (FSK), phase shift-keying (PSK), orthogonal frequency division multiplexing (OFDM), or variations  
35 thereof. As is also known, Bluetooth utilizes an FSK

modulation/demodulation protocol, while IEEE 802.11a and IEEE 802.11b utilize OFDM and/or a form of PSK for its modulation/demodulation protocol.

5        Regardless of the particular modulation/demodulation protocol, a radio receiver generally includes an antenna section, a filtering section, a low noise amplifier, an intermediate frequency (IF) stage, and a demodulator. In operation, the antenna section receives RF modulated  
10 signals and provides them to the filtering section, which passes RF signals of interest to the low noise amplifier. The low noise amplifier amplifies the received RF signals of interest and provides them as amplified RF signals to the IF stage. The IF stage includes one or more local  
15 oscillators, one or more mixers, and one or more adders to step-down the frequency of the RF signals of interest to an intermediate frequency or to base-band. The IF stage provides the intermediate frequency signals or base-band signals to the demodulator, which, based on the  
20 demodulation protocol, recaptures the data.

A demodulator may be implemented using analog and/or digital circuitry. Digital demodulators are generally better suited for use in an integrated circuit (IC) radio  
25 receiver than analog demodulators because of reduced sensitivity to noise and less IC real estate intensive. Such demodulators typically require high order low pass filters and sophisticated DC offset correction circuitry.

30        Such high order low pass filters are typically required to pass the frequencies of interest and sharply attenuate other frequencies (e.g., at a rate of -

60dB/decade). To achieve such a large roll-off, digital high order low pass filters require a significant amount of logic circuits including multipliers.

5 For FSK demodulation, such as used in Bluetooth, the DC offset correction circuitry corrects for frequency differences between the local oscillations of IF stage in the transmitter section of a sending radio and in the receiver section of the receiving radio. Presently, such  
10 DC offset correction circuitry performs peak and valley detection to identify a peak and valley. From these values a DC value is determined (e.g., typically a midpoint between the peak and valley). The peak and valley values are continuously updated, thus the DC value is also  
15 continually updated. While this continuous updating allows for fast and continuous correction of the DC offset value, such circuitry is subject to false peak and/or valley detection. When a false peak or valley is detected, an error results in the DC value, which adversely affects the  
20 performance of a wireless radio.

Therefore, a need exists for a reliable, low cost, reduced complexity, and reduced integrated circuit real estate digital demodulator for use in integrated circuit  
25 radios and/or integrated circuit radio receivers.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1 illustrates a schematic block diagram of a  
30 radio receiver in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of an alternate radio receiver in accordance with the present invention;

5        Figure 3 illustrates a schematic block diagram of a further alternate radio receiver in accordance with the present invention;

10        Figure 4 illustrates a schematic block diagram of yet another radio receiver in accordance with the present invention;

15        Figure 5 illustrates a schematic block diagram of the mixing module utilized in the radio receivers of Figures 1 through 3;

20        Figure 6 illustrates a schematic block diagram of a digital demodulator that may be utilized in one or more of the radio receivers in Figures 1 through 4;

25        Figure 7 illustrates a schematic block diagram of a low pass filter/equalizer that may be utilized in the digital demodulator of one or more of the radio receivers of Figures 1 through 4;

      Figure 8 illustrates a frequency response of the low pass filter/equalizer of Figure 7;

30        Figure 9 illustrates a logic diagram of a method for digital demodulation in accordance with the present invention;

Figure 10 illustrates a graphical diagram of a Bluetooth packet that may be processed by a radio receiver in accordance with the present invention;

5        Figure 11 illustrates a graphical representation of DC offset correction in accordance with the present invention;

Figure 12 illustrates a logic diagram that further describes Step 192 of Figure 9;

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Figure 13 illustrates a logic diagram of a method that further describes the determination of a peak value at Step 220 of Figure 12;

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Figure 14 illustrates a logic diagram of a method that further describes the determination of a valley value of Step 224 of Figure 12;

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Figure 15 illustrates a logic diagram that expands on the logic diagram of Figure 12 by detecting false peaks and false valleys in accordance with the present invention;

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Figure 16 illustrates a logic diagram of a method that expands on the logic diagram of Figure 12 by detecting peaks and valleys in accordance with the present invention;

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Figures 17 and 18 illustrate a graphical representation of determining peak and valley values during acquisition mode and tracking mode in accordance with the present invention;

Figure 19 illustrates a logic diagram that further describes Step 196 of Figure 9;

Figure 20 illustrates a logic diagram that further describes Step 296 of Figure 19;

Figure 21 illustrates a logic diagram of a method for adjusting the sampling position in accordance with the present invention; and

Figure 22 illustrates a graphical representation of the sampling of a data packet in accordance with the present invention.

#### DETAIL DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides a digital demodulator that may be utilized in integrated radio receivers and/or integrated radios. The digital demodulator may be implemented in a variety of embodiments. One embodiment includes a mixing section, 1<sup>st</sup> and 2<sup>nd</sup> digital comb filters, phase locked loop module, and a data recovery module. The mixing section is operably coupled to produce a digital I signal and a digital Q signal from a digital intermediate frequency signal. The 1<sup>st</sup> comb filter filters the digital I signal while the 2<sup>nd</sup> comb filter filters the digital Q signal. The phase locked loop module produces a digital signal from the filtered I and filtered Q signals. The data recovery module interprets the digital signal to recapture a data stream.

In another embodiment, the digital demodulator includes a mixing section, phase locked loop module, and data recovery module. The data recovery module includes a DC offset module and a data extraction module. The mixing section produces a digital I signal and digital Q signal, which are processed by the phase locked loop module to produce a digital signal. The DC offset module, based on a DC offset value, adjusts the digital signal to produce a DC adjusted digital signal. The data extraction module processes the DC adjusted digital signal to recapture a data stream.

In yet another embodiment, the digital demodulator includes a mixing section, a phase locked loop, a low pass filter/equalizer, and a data recovery module. In this embodiment, the phase locked loop produces the digital signal from a digital I and digital Q signal, which are produced by the mixing section. The low pass filter/equalizer equalizes the digital signal and then utilizes a comb filter function to produce a filtered and equalized digital signal. The data recovery module processes the filtered and equalized digital signal to recapture a data stream. With such a variety of digital demodulator implementations, a digital demodulator is readily achieved that is reliable, low cost, has reduced integrated circuit real estate requirements, and has reduced circuit complexity requirements.

The present invention can be more fully described with reference to Figures 1 through 22. Figure 1 illustrates a schematic block diagram of a radio receiver 10 that includes a low noise amplifier 12, an intermediate

frequency (IF) mixing module 14, and a digital demodulator 16. The digital demodulator 16 includes a mixing section 18, a 1<sup>st</sup> digital comb filter 20, a 2<sup>nd</sup> digital comb filter 22, a phase locked loop module 24 and a data recovery module 26. The low noise amplifier 12 is operably coupled to receive a radio frequency (RF) signal 28. The RF signal 28 may be representative of a wireless communication that utilizes a particular wireless standard such as Bluetooth, IEEE 802.11a, IEEE 802.11b, et cetera. The low noise amplifier 12 amplifies the RF signal 28 to produce an amplified RF signal 30.

The IF mixing module 14, which will be described in greater detail with reference to Figure 5, mixes the amplified RF signal 30 with a local oscillation 32 to produce a digital IF signal 34. For example, if the RF signal 28 is in accordance with the Bluetooth standard, the carrier frequency is approximately 2.402 GHz. If the local oscillation 32 is 2.400 GHz, the resulting frequency of the digital IF signal 34 is 2 MHz. The digital IF signal 34 includes an I component and a Q component, where the I component represents the in-phase portion of the digital IF signal and the Q component represents the quadrature portion of the digital IF signal 34.

The mixing section 18, which will be described in greater detail with reference to Figure 6, receives the digital IF signal 34 and produces a digital Q signal 36 and a digital I signal 38, both of which are at base-band. Accordingly, the mixing section 18 includes a local oscillation, which down converts the frequency of the digital IF signal 34 to base-band.



The digital comb filter 20 filters the digital I signal 38 to produce a filtered I signal 42. The digital comb filter 22 filters the digital Q signal 36 to produce a filtered Q signal 40. The 1<sup>st</sup> and 2<sup>nd</sup> digital comb filters 20 and 22 are designed using a plurality of delays and corresponding taps to provide a frequency response that has notches at the frequencies which substantially correspond to frequencies of interfering channels of the RF signal.

For example, if the RF signal 28 is in accordance with the Bluetooth standard, the interfering channels will be at 1 MHz increments from the frequency of the desired channel. Accordingly, the digital comb filters 20 and 22 are constructed such that the notches of the frequency response correspond to the 1 MHz increments. By utilizing such digital comb filters to provide a low pass filter function, less circuitry is required to implement the low pass filter.

The phase locked loop (PLL) module 24 receives the filtered I signal 42 and the filtered Q signal 40 and produces therefrom a digital signal 44. The phase locked loop module 24, which will be discussed in greater detail with reference to Figure 6, generally performs a frequency to amplitude conversion on the I and Q signals 40 and 42. As such, the digital signal 44 is an amplitude representation of the frequencies corresponding to the filtered I signal 42 and filtered Q signal 40. As is known, if the modulation scheme is frequency shift keying, a 0 is represented by a first carrier frequency and a logic 1 is represented by a second carrier frequency. For

example, Bluetooth utilizes 2.402 GHz minus 160 KHz for a logic 0 and 2.402 GHz plus 160 KHz for a logic 1.

The data recovery module 26, which will be described in greater detail with reference to Figure 6, receives the digital signal 44 and recaptures a data stream 46 therefrom. The data recovery module 26, when needed, performs a DC offset of the digital signal and then interprets the resulting waveform to recapture the data that comprises the data stream 46.

Figure 2 illustrates a schematic block diagram of a radio receiver 50 that includes the low noise amplifier 12, the IF mixing module 14, and a digital demodulator 52. The low noise amplifier 12 and IF mixing module 14 function as previously described with reference to Figure 1.

The digital demodulator 52 includes a mixing section 19, the phase locked loop module 24, and a data recovery module 54. The data recovery module 54 includes a DC offset module 56 and a data extraction module 58. The mixing section 19, which will be described in greater detail with reference to Figure 6, receives the digital IF signal 30 and produces base-band digital Q signal 37 and base-band digital I signal 39. The phase locked loop module 24 receives the digital Q signal 37 and digital I signal 39 and produces the digital signal 44.

The DC offset module 56 receives the digital signal 44 and determines a DC offset 60 therefrom. The DC offset module 56 utilizes a 1<sup>st</sup> criteria to determine the DC offset when the radio receiver is in an acquisition mode and uses

a 2<sup>nd</sup> criteria to determine the DC offset when the radio receiver is in the tracking mode. Having determined the DC offset 60, the DC offset module 56 removes the DC offset 60 from the digital signal 44 to produce a DC adjusted digital signal 62. As one of average skill in the art will appreciate, the DC offset 60 is a result of the difference in local oscillator frequencies utilized in the transmitter section of a transmitting radio and the local oscillation 32 of radio receiver 50 in the receiving radio. As one of average skill in the art will further appreciate, if the DC offset is not properly accounted for, the ability to accurately extract data from the digital signal is severely impacted. As such, the DC offset 60 needs to be accurately and reliably determined to ensure the accurate extraction of data.

The data extraction module 58 samples the DC adjusted digital signal 62 at a sampling rate to produce samples of the signal. The samples are then interpreted to produce data that comprises the data stream 46. The functionality of the DC offset module and data extraction module will be discussed in greater detail with reference to Figures 9 through 22.

Figure 3 illustrates a schematic block diagram of radio receiver 70 that includes the low noise amplifier 12, the IF mixing module 14, and a digital demodulator 72. The functionality of the low noise amplifier 12 and IF mixing module 14 are as previously discussed with reference to Figure 1.

The digital demodulator 72 includes the mixing section 19, a phase locked loop 25, a low pass filter/equalizer 74 and the data recovery module 26. The mixing section 19, which functions as previously described with reference to Figure 2, produces a base-band digital Q signal 37 and a base-band digital I signal 39. The phase locked loop 25 receives the digital I and digital Q signals 37 and 39 and performs a frequency to amplitude conversion thereon to produce digital signal 44.

The low pass filter/equalizer 74, which will be discussed in greater detail with reference to Figures 7 and 8, includes a combined equalizing and low pass filtering function. The low pass filter/equalizer 74 equalizes and low pass filters the digital signal 44 to produce an equalized and filtered digital signal 82.

The data recovery module 26, which functions as previously described with reference to Figure 1, receives the filtered digital signal 82 and produces therefrom a data stream 46.

Figure 4 illustrates a schematic block diagram of radio receiver 90 that includes the low noise amplifier 12, an IF mixing module 102, a polyphase filter 104, a limiting module 110, an analog to digital converter 112 and a digital demodulator 92. The digital demodulator 92 includes a mixing section 95, the phase locked loop module 24, and the data recovery module 26.

The low noise amplifier 12 receives the RF signal 28 and produces therefrom the amplified RF signal 30. The IF

mixing module 102 mixes the amplified RF signal 30 and the local oscillation 32 to produce an IF Q signal 106 and an I IF signal 104. The IF mixing module 102 may include a pair of mixers to mix the quadrature component of amplified RF  
5 signal 30 with the quadrature component of local oscillation 32 to produce the IF Q signal 106. In addition, the IF mixing module 102 may include another mixer that mixes the in-phase component of the amplified RF signal 30 with the in-phase component of the local  
10 oscillation 32 to produce IF I signal 104.

The polyphase filter 108 is operably coupled to receive the IF Q signal 106 and the IF I signal 104. The polyphase filter performs a band-pass function that filters  
15 the images produced by the IF mixing module such that only the desired tones remain for the filtered I signal 104 and filtered Q signal 116. For a further discussion on the operation of the polyphase filter 108 refer to co-pending patent application entitled XX, having a serial number of  
20 XX, and a filing date of XX.

Since the polyphase filter 108 rejects the images, only the filtered I signal 114 is utilized to extract the data stream 46. To do this, the limiting module 110 limits  
25 the magnitude of the filtered I signal 114 to produce a limited I signal 118. In essence, the limiting module 110 is taking a sinusoidal waveform (i.e., the filtered I signal 114) and producing a square wave representation thereof (i.e., the limited I signal 118).

The analog to digital converter 112 receives the limited I signal 118 and produces a digital I signal 120

therefrom. The analog to digital converter 112 may be a continuous time Sigma Delta analog to digital converter that is of a 2<sup>nd</sup> order and has a quantizing frequency of 24 MHz. In addition, the digital I signal 120 may be a 2-bit value that is provided to the digital demodulator 92.

The mixing section 95 of digital demodulator 92 receives the digital I signal 120 and mixes it with a reference Q signal 96 and a reference I signal 94 to produce a digital base-band Q signal 98 and a digital base-band I signal 100. The reference I and Q signals 94, 96 may be provided by a local oscillator. The phase locked loop module 24 receives the digital base-band Q signal 98 and digital base-band I signal 100 and produces therefrom the digital signal 44. The data recovery module 26 interprets the digital signal 44 to produce the data stream 46.

Figure 5 illustrates a schematic block diagram of the IF mixing module 14 of the radio receivers illustrated in Figures 1 through 3. The IF mixing module 14 includes an image rejection mixer that includes an I mixer 132, a Q mixer 134, a band-pass filter 140, a limiter 142, and an analog to digital converter 144.

In operation, the amplified RF signal 30 (e.g., a  $\cos(\omega_{\text{RF}}t)$ ) is received by the IF mixing module 14. The amplified RF signal 30 is mixed with a Q local oscillation 148 (e.g.,  $\cos(\omega_{\text{IF}}t)$ ) via Q mixer 134 to produce an IF Q signal 152. The amplified RF signal is also passed through a minus 90 degree phase shift module 130 to produce a phase shifted RF signal (e.g.,  $\sin(\omega_{\text{RF}}t)$ ). The phase shifted RF

signal is mixed with an I local oscillation 146 (e.g.,  $\sin(\omega_{IFT})$ ) via mixer 132 to produce IF I signal 150.

The band pass filter 140 filters the IF I signal 150 and IF Q signal 152 to substantially eliminate image tones and other undesired tones to produce a filtered IF signal 156. Note that the band pass filter 140 may only filter one of the IF I signal 150 and the IF Q signal 152 if the filter 150 is a poly-phase filter. The limiter 142 receives the filtered IF signal 156, which may include an I component and/or a Q component, and limits the amplitude to produce a limited IF signal 158, which will include an I component and/or a Q component. In essence, the limiter 142 is converting the sinusoidal waveform of the filtered IF signal 156 into a square wave signal (i.e., the limited IF signal 158). The analog to digital converter 144 converts the limited IF signal 158 into the digital IF signal 34.

Figure 6 illustrates a schematic block diagram of a digital demodulator 16, 52, 72, and/or 92. The demodulator includes mixing section 19 or 95, the phase locked loop module 24 and the data recovery module 26 or 54. The mixing section 19 or 95 includes mixing section 18, low pass filter 166 and low pass filter 168. The low pass filters 166 and 168 may be implemented utilizing a comb filter wherein the notches of the comb filter are set at frequencies corresponding to undesired tones and/or channels of the received RF signal 28.

The mixing section includes a direct digital frequency synthesizer 160, a 1<sup>st</sup> mixing module 162 and a 2<sup>nd</sup> mixing

module 164. The direct digital frequency synthesizer (DDFS) produces a local oscillation having an in-phase component (e.g.,  $\cos \omega_0 t$ ) and a quadrature local oscillation (e.g.,  $-\sin \omega_0 t$ ). Accordingly, mixer 162 mixes the in-phase  
 5 local oscillation with the in-phase component of the digital IF signal 34 or the digital I signal 120 to produce a base-band I signal. The mixer 164 mixes the quadrature local oscillation produced by DDFS 160 with the digital IF signal 34 or the digital I signal 120 to produce a  
 10 quadrature component to produce a base-band Q signal.

The low pass filters 166 and 168 filter the corresponding I and Q signals, which are then provided to the phase locked loop module 24. As one of average skill  
 15 in the art will appreciate, the mixing section 18 may be implemented utilizing a state machine that is operably coupled to frequency shift, by a factor of N and phase shift by a factor of  $(\pi/2)$  the digital IF signal to produce the I signal and to frequency shift, by the factor of N and  
 20 phase shift by  $(-\pi)$  the digital IF signal to produce the digital Q signal.

The phase locked loop module 24 includes the phase locked loop 25, a tapped delay line 172, and the low pass  
 25 filter/equalizer 74. The phase locked loop 25 receives the filtered I and Q signals from the mixing section 19 or 95 and performs a frequency to amplitude conversion thereon. The resulting signal is provided to the tapped delay line 172, which, based on a delay select signal 178, outputs the  
 30 signal from the phase locked loop 25 with a desired delay. The delaying of the output of the phase locked loop 25 will be discussed in greater detail with reference to Figures 17



through 22. In general, the delaying of the output of the phase locked loop 25 is used to better align the signal with the data extraction module to enhance the reliability of data extraction.

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The data recovery module 26 or 54 includes a processing module 174 and memory 176. The processing module 174 may be a single processing device or a plurality of processing devices. Such a processing device may be a

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microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions.

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The memory 176 may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static memory, dynamic memory, flash memory, and/or any device that stores digital information. Note that when

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the processing module 174 implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding operational instructions is embedded with the circuitry comprising the state machine or logic circuitry. The memory 176 stores and the

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processing module 174 executes at least some of the operational instructions described in with reference to Figures 9 through 22.

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The data recovery module 26 or 54 implements the DC offset module 56 and data extraction module 58 to accurately recapture the data stream 46. The general functionality of the DC offset module 56 and data

extraction module 58 were previously discussed with reference to Figure 2 and will be described in greater detail with reference to Figures 9 - 22.

Figure 7 illustrates a schematic block diagram of the low pass filter/equalizer 74. The low pass filter/equalizer 74 includes digital logic circuitry, summing module, a 1<sup>st</sup> comb filter 180, and a 2<sup>nd</sup> comb filter 182. The 1<sup>st</sup> comb filter 180 is a 12-tap filter that provides notches at 1 MHz intervals while the 2<sup>nd</sup> comb filter 182 is an 8-tap filter that provides notches at 1.5 MHz intervals. The frequency step-down converter 184 steps down the frequency of the filtered signal by a factor of 2.

Figure 8 illustrates a graphical representation of the frequency response of the low pass filter/equalizer 74 of Figure 7. The equalizer 76 provides an equalized response 186, which provides gain in the frequency range from 0 to 1 MHz. The comb filter 78 provides the low pass filtering response 188. The 1st comb filter 180 provides the notches at 1, 2, 3, 4, 5 and 6 MHz. The 2nd comb filter 182 provides the notches at 1.5, 3, 4.5, and 6 MHz. As such, by positioning the notches of comb filters 180 and 182 at frequencies of undesired channels and images, a simple comb filter may be utilized in place of a high order low pass filter to obtain the same desired low pass filter response. As such, a digital demodulator that utilizes comb filters in this manner as opposed to high order low pass filters is less complex, thus requires less integrated circuit real estate and is less costly.

Figure 9 illustrates a logic diagram of a method for digital demodulation in accordance with the present invention. The processing begins at Step 190 where a digital signal is received. The digital signal is  
 5 representative of a received RF signal that has been amplified, frequency down converted, comb filtered, and frequency to amplitude converted. For example, the received RF signal is amplified to produce an amplified RF signal. The amplified RF signal is then mixed with a local  
 10 oscillation to produce a digital IF signal. The digital IF signal is then mixed with a synthesized frequency to produce a digital baseband Q signal and a digital baseband I signal. The digital baseband Q signal and digital baseband I signal are then comb filtered and processed by a  
 15 phase locked loop to produce the digital signal.

Alternatively, the digital signal may be produced by amplifying an RF signal and then mixing the amplified RF signal with a local oscillation to produce a digital IF  
 20 signal. The digital IF signal is then mixed with a reference I signal and a reference Q signal to produce a digital baseband I signal and a digital baseband Q signal. The digital baseband I signal and digital baseband Q signal are processed by a phase locked loop to produce a digital  
 25 base-band signal. The digital base-band signal may be equalized and then comb filtered to produce the digital signal.

The process then proceeds to Step 192 where a DC  
 30 offset is determined utilizing a 1<sup>st</sup> criteria when a radio receiver is in an acquisition mode and using a 2<sup>nd</sup> criteria when the radio receiver is in a tracking mode. The

determination of the DC offset will be described in greater detail with reference to Figures 10 through 18.

The process then proceeds to Step 194 where the DC  
5 offset is substantially removed from the digital signal to produce a DC adjusted digital signal. The process then proceeds to Step 196 where the DC adjusted digital signal is sampled at a sampling rate to produce a data stream. The sampling of the DC adjusted digital signal will be  
10 described in greater detail with reference to Figures 19 through 22.

Figure 10 illustrates a Bluetooth packet 200 that includes a preamble 201, a synchronization word 202, a  
15 trailer word 203, and data 204. The Bluetooth packet 200 is modulated in accordance with an FSK modulation scheme and correspondingly demodulated via the radio receiver of the present invention. As shown, the preamble 201 (e.g., first 4 bits), the synchronization word 202 (e.g., next 64  
20 bits), and the trailer word 203 (e.g., next 3 bits), correspond to the acquisition mode for a Bluetooth packet 200. The tracking mode includes the data section 204 and ends at the end of the packet 200.

25 Since the acquisition mode is relatively short, the 1<sup>st</sup> criteria for determining the DC offset must occur very quickly to obtain a good estimation for the DC offset. During the tracking mode, which includes the data 204, the DC offset is fine tuned utilizing the 2<sup>nd</sup> criteria. As  
30 such, the 1<sup>st</sup> criteria allows for rapid adjustments in the DC offset while the 2<sup>nd</sup> criteria allows for less dramatic changes in the DC offset.

Figure 11 illustrates a graphical representation of the beginning of Bluetooth packet 200 as the digital signal 44, which is outputted from the PLL module 24. Prior to the reception of the packet, noise 206 is being received. At the commencement of the packet, which corresponds to packet data 208, the DC offset 210 is determined with respect to a zero DC level 212 and a zero reference 211. The zero reference 211 corresponds to a midpoint of the dynamic range of the digital demodulator while the zero DC level 212 corresponds to the midpoint of the data. The DC offset is the difference between the zero reference 211 and the zero DC level 212. In general, to remove the DC offset, the zero DC level 212 needs to be shifted to align with the zero reference 211. The determination of the DC offset and correcting the digital signal to remove the DC offset is further described with reference to Figures 12 through 18.

Figure 12 illustrates a logic diagram for determining the DC offset. The process begins at Step 220 where a peak value of the digital signal is determined based on a current peak value, a previous peak value and the 1<sup>st</sup> or 2<sup>nd</sup> criteria. Such a determination will be described in greater detail with reference to Figures 13, 17 and 18.

The process then proceeds to Step 224 where a valley value of the digital signal is determined based on a current valley value, a previous valley value, and the 1<sup>st</sup> or 2<sup>nd</sup> criteria. This processing will be described in greater detail with reference to Figures 14, 17 and 18.

The process then proceeds to Step 226 where the DC offset is determined based on the peak value and the valley value. Typically, the DC offset represents the difference between the zero reference 211 (Figure 11) and the center point of the peak value and the valley value.

Figure 13 illustrates a logic diagram for determining the peak value. The process begins at Step 228 where a determination is made as to whether the radio receiver is in the acquisition mode or tracking mode. If the radio receiver is in the acquisition mode, the process proceeds to Step 232 where a determination is made as to whether the magnitude of the current peak value is greater than the magnitude of the previous peak value. If so, the process proceeds to Step 234 where the current peak value is stored as the peak value. Thus, in the acquisition mode (e.g., using the 1<sup>st</sup> criteria) on a peak-by-peak basis, if the current peak is greater than the previous peak, the current peak value will be used as the peak value. The process then reverts to step 228.

If the magnitude of the current peak value is not greater than the magnitude of the previous peak value, the process proceeds to Step 230. At Step 230, the peak value is determined as a result of the previous peak value less a peak acquisition delta value multiplied by a difference of the current peak value and the previous peak value, wherein the 1<sup>st</sup> criteria indicates a greater value for the peak acquisition delta value than the 2<sup>nd</sup> criteria. In general, if the magnitude of the current peak value is not greater than the magnitude of the previous peak value, the peak value will be exponentially decreased based on the

difference between the current peak value and the previous peak value. In general, the determination of the peak value may be done in accordance with the equation:  $PV(n) = PV(n-1) \pm [dP \cdot \text{abs}(PV(c) - PV(n-1))]$ , wherein  $PV(n)$  is the peak value,  $PV(n-1)$  is the previous peak value,  $dP$  is the peak acquisition delta value, and  $PV(c)$  is the current peak value

If the radio receiver is in the tracking mode, the peak value is determined as described at Step 229. At Step 229, the peak value is not instantaneously adjusted from peak-to-peak but exponentially changed at a much slower rate than when in acquisition mode. This may be done by using the equation  $PV(n) = PV(n-1) \pm dP$ , wherein  $PV(n)$  is the peak value,  $PV(n-1)$  is the previous peak value and  $dP$  is the peak acquisition delta value. Based on this equation, if the current peak value is greater than the peak value, the  $dP$  term is added to the peak value. If the current peak value is less than the peak value, the  $dP$  term is subtracted from the peak value.

Figure 14 illustrates a logic diagram for determining the valley value. The process begins at Step 236 where a determination is made as to whether the radio receiver is in acquisition mode or tracking mode. When in acquisition mode, the process proceeds to Step 240 where a determination as to whether the absolute value of the magnitude of the current valley is greater than the absolute value of the magnitude of the previous valley. If so, the process proceeds to Step 242 where the current valley value is stored as the valley value. As such, from valley to valley if the magnitude of the current valley is

greater than the magnitude of the previous valley in acquisition mode, the current valley will be used as the valley value to determine the DC offset. The process then reverts to step 236.

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If the magnitude of the current valley value is not greater than the magnitude of the previous valley value, the process proceeds to Step 238. At Step 238, the valley value is determined based on the 1<sup>st</sup> criteria during the acquisition mode, which utilizes a greater exponential determination decrementing of the valley value from the previous valley value to the current valley value. For example, the degradation may be  $\frac{1}{2}$ . As such, if the previous valley value was 1 and the current valley value is 0.5, the valley value that will be used is 0.75. In general for acquisition mode, the valley value is determined in accordance with the equation  $VV(n) = VV(n-1) \pm [dV \cdot \text{abs}(VV(c) - VV(n-1))]$ , wherein  $VV(n)$  is the valley value,  $VV(n-1)$  is the previous valley value,  $dV$  is the valley acquisition delta value, and  $VV(c)$  is the current valley value. Based on this equation, if the current valley value is greater than the valley value, the  $[dV \cdot \text{abs}(VV(c) - VV(n-1))]$  is added to the absolute value of the magnitude of the valley value. If the current valley value is less than the valley value, the  $[dV \cdot \text{abs}(VV(c) - VV(n-1))]$  is subtracted from the absolute value of the magnitude of the valley value.

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If the radio receiver is in the tracking mode, the valley value will be determined at Step 237. In this mode, the valley value will be adjusted based on an exponential change factor. The exponential change factor will be



significantly smaller than when in the acquisition mode. For example, if the change factor for the acquisition mode is 0.5, the change factor in the tracking mode may be 0.05. In general, the valley value is determined in accordance

5 with the equation  $VV(n) = VV(n-1) \pm dV$ , wherein  $VV(n)$  is the valley value,  $VV(n-1)$  is the previous valley value, and  $dV$  is the valley acquisition delta value. Based on this equation, if the current valley value is greater than the valley value, the  $dV$  term is added to the absolute value of

10 the magnitude of the valley value. If the current valley value is less than the valley value, the  $dV$  term is subtracted from the absolute value of the magnitude of the valley value.

15 Figure 15 illustrates a logic diagram for detecting false peaks and false valleys. The detection of a false peak is described in Steps 250-256. The detection of false valleys is described in Steps 258-264. At Step 250, a potential peak valley of the digital signal is detected.

20 The process then proceeds to Step 252 where the magnitude of the potential peak is determined. The process then proceeds to Step 254 where a difference between the magnitude of the potential peak and the magnitude of a valley value is determined. The process then proceeds to

25 Step 256 where, when the difference is less than a predetermined value, the potential peak is identified as a false peak.

30 At Step 258, a potential valley of the digital signal is detected. The process then proceeds to Step 260 where the magnitude of the potential valley is determined. The process then proceeds to Step 262 where a difference

between the magnitude of the potential valley and the magnitude of the peak valley is determined. The process then proceeds to Step 264 where, when the difference is less than a predetermined value, the potential valley is  
 5 identified as a false valley.

Figure 16 illustrates a logic diagram of a method for detecting peaks and valleys. The process begins at Step 266 where a gradient of the digital signal is determined.  
 10 The process then proceeds to Step 268 of Step 272. At Step 268 a determination is made as to when the gradient changes from a positive to a negative. The process then proceeds to Step 270 where the digital signal is indicated as being at a peak when the gradient changes from positive to  
 15 negative.

At Step 272 a determination is made as to when the gradient changes from negative to positive. The process then proceeds to Step 274 where the digital signal is  
 20 indicated as being at a valley when the gradient changes from positive to negative. As one of average skill in the art will appreciate, the determination of gradient of a digital signal utilizing digital logic may be done by a differential function that may be easily implemented  
 25 utilizing delay modules to achieve the desired differentiation. As such, only the sign of the derivative function needs to be analyzed to determine whether a peak or valley is being identified.

30 Figure 17 illustrates a graphical representation of determining the peak value 280 and the valley value 282 during the acquisition mode. As shown, the packet data 208

varies from multiple levels to other levels. In this illustration, the gradient on the 1<sup>st</sup> pulse of packet data 208 changes from a positive slope to a negative slope thus indicating a peak. Since this is the 1<sup>st</sup> peak during the acquisition mode, this value is stored as peak value 280. The gradient of the packet data 208 is continually monitored until it changes from a negative value to a positive value. This value is then used as the valley value 208. At this point in time, the DC offset may be determined as the midway point between the peak value 280 and the valley value 282.

At the next peak, since the peak is greater than the previous peak, the peak value 280 is adjusted to the magnitude of the current peak. Following the waveform, the next valley of packet data 208 is less than the previous valley value. As such, the valley value 282 is reduced based on a valley acquisition delta value of the difference between the previous valley value and the current valley value. In this example, the delta value is 50%.

Continuing with the waveform, the next peak has a magnitude that is less than the previous peak. As such, the peak value 280 is adjusted down by the peak acquisition delta value, which, for this example, is  $\frac{1}{2}$  of the difference between the current peak value and the previous peak value for this example.

The waveform then proceeds to the next valley point, which has a greater magnitude than the valley value 282 at that point. As such, the valley value 282 is adjusted to correspond to the magnitude of the current valley.

The next peak includes a false valley value 284. As shown, the gradient detection identifies a peak at the beginning of the pulse, which would cause the peak value 280 to be adjusted to that level since it is greater than the peak value at this point. The gradient detection circuitry would then identify the point, which has been identified as a false valley value 284, as being the next current valley value. Since the difference between the value of the potential next current valley value and the peak value 280 falls below a threshold (which may be set based on the known peak and valley values), this point is identified as a false valley. Similarly, a few pulses further in time, a false peak value 286 is identified during a valley pulse.

Figure 18 illustrates the data packet 208 during the tracking mode. The processing is very similar to the processing described with reference to Figure 17 other than the peak value and valley values 280 and 282, respectively, change at a much slower rate and independently of the magnitude of difference between the current value and the stored value. As shown, the peak value 280 and valley value 282 do not rapidly adjust as the peak and valley values of current pulses change. This results because the 2<sup>nd</sup> criteria for determining these values has a valley acquisition delta value and peak acquisition delta value that are significantly less than during the acquisition mode.

Figure 19 illustrates a logic diagram for the sampling of the DC adjusted signal as generally described at Step

196 of Figure 9. The process begins at Step 290 where the DC adjusted signal is over sampled at the sampling rate. The process then proceeds to Step 292 where alternating ones of the samples are correlated over a plurality of bits that correspond to the synchronization word of the current packet being processed. For example, if the over sampling rate is 6, the alternating sample points of 0, 2, and 4, or 1, 3, 5 of the DC adjusted digital signal may be correlated with the known synchronization word.

The process then proceeds to Step 294 where one of the correlated sample sets is identified as having the best correlation with the synchronzation word. For example, each pulse of the DC adjusted digital signal is sampled 6 times. Three of these samples are correlated. The correlated results are then compared with the known synchronization word. The correlated sets of samples that best matches the known synchronization word is the one identified at Step 294.

The process then proceeds to Step 296 where a sampling position of the over sampling of the DC adjusted digital signal is selected based on the identified correlated sampling set. For example, if it is determined that the 2<sup>nd</sup> over sampling position produces the best correlation with the synchronization word, then the 2<sup>nd</sup> sampling position will be utilized to sample the digital signal word to accurately retrieve the desired digital information.

The process then proceeds to Step 298 where samples at the selected sample position are utilized to produce the data stream.

Figure 20 illustrates a logic diagram for selecting the particular sampling position. This begins at Step 300 where adjacent sample sets are compared to the identified correlated sample set with respect to a typical waveform of the DC adjusted signal to determine an over sampling relationship of the DC adjusted digital signal. The process then proceeds to Step 302 where the sampling position is selected to be the sampling position that provides the identified correlated sample set when the sampling that produces the identified correlated sampling set occurs at a most favorable point of the over sampling relationship (e.g., sampling point 2). The process then proceeds to Step 304 where the sampling position is selected to be the sampling between the identified correlated sampling set and an adjacent one of the plurality of correlated sampling sets when the sampling between the identified correlated sampling set and an adjacent one correlated sampling sets occurs at a most favorable point of the over sampling relationship (e.g., sample point 3, when sampling points 2 and 4 were correlated). The sampling described in Figures 19 and 20 will be described graphically with reference to Figure 22.

Figure 21 illustrates a logic diagram that adjusts the sampling position via the tapped delay line 172 of the phase locked loop module 24. The process begins at Step 310 where a 1<sup>st</sup> reference sample is obtained prior to the sampling of the DC adjusted signal. The process then proceeds to Step 312 where a 2<sup>nd</sup> reference sample is obtained subsequent to the data sampling of the DC adjusted digital signal. The process then proceeds to Step 314

where over a plurality of sampling of the DC adjusted digital signals a difference between the 1<sup>st</sup> and 2<sup>nd</sup> reference samples are accumulated to produce an accumulated difference. The process then proceeds to Step 316 where  
5 the sampling is adjusted when the accumulated difference overflows an upper threshold or when the accumulated difference underflows a lower threshold.

Figure 22 illustrates a graphical representation of  
10 the processing described in Figures 19 through 21. As shown, a data packet 208 is over sampled at 6 times the data rate. Of the 6 over sampling points, only 3 per data rate are used to produce the correlated sample sets. As shown in this example, correlated sample set that occurs  
15 with the 0<sup>th</sup> over sampling, 2<sup>nd</sup> over sampling, and 4<sup>th</sup> over sampling are utilized. As such, correlated sample sets 0, 2 and 4 are the sample sets being referenced in Step 292 of Figure 19.

20 The particular sampling point, which corresponds to one of the 6 over sampling positions, is determined in the 1<sup>st</sup> pulse based on the known wave shape of the data packet. In essence, the known wave shape of the data packet is a rounded square wave. As such, it will have a particular  
25 peak and a particular valley as graphically shown. For the 1<sup>st</sup> interval, the correlated sample set 2 and correlated sample set 4 will accurately represent the data such that the correlation to the synchronization word may be readily obtained. However, as shown, the peak of the 1<sup>st</sup> pulse  
30 actually occurs more closely in time with the 3<sup>rd</sup> sampling interval. Thus, as described in Figure 20, the 3<sup>rd</sup> sampling interval would be selected since based on the known

relationship of the data packet, point 3 would occur at a larger magnitude than points 2 or 4, thus providing a better sampling point.

At some point later in time, and for this example as shown as the 3<sup>rd</sup> data pulse, the 4<sup>th</sup> sampling set has a magnitude greater than the 2<sup>nd</sup> or 0<sup>th</sup> sampling points. As such, as also described in Figure 20 at Step 302, point 4 would be used as the sampling interval since based on the known wave shape of the data packet, the magnitude at point 4 is greater than the magnitude at point 2. Thus, the magnitude at point 4 is most likely the greatest magnitude of the data packet.

The processing described in Figure 21 allows for the over sampling intervals to be time shifted left or right with relationship to the data packet 208 to better position the sampling intervals with the peak of the waveform. The time adjustment may shift the data packet 208, with respect to the over sampling intervals such that the peak either occurs at 2 or 4 or at over sampling point 3. For example, the 1<sup>st</sup> pulse shown in the waveform of data packet 208 has its peak occurring exactly at the 3<sup>rd</sup> over sampling point. As such, the timing of the sampling is very good. If, however, the peak of the waveform occurred between sampling intervals 2 and 3, the over sampling rate may be delayed with respect to the packet data 208 such that the peak either occurs at over sampling point 2 or over sampling point 3.

The preceding discussion has presented a method and apparatus for digital demodulation that may be utilized in



an integrated radio receiver. By utilizing comb filters, low pass filters/equalizers and DC offset circuitry as previously described, a digital demodulator that is reliable, cost efficient (i.e., real estate efficient) is readily obtained. As one of average skill in the art will appreciate, other embodiments may be derived from the teachings of the present invention, without deviating from the scope of the claims.

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[illegible]